Page 2, lines 2-22, delete current paragraphs and insert therefor:

The present invention is made to solve the problem described above, and an object thereof is to provide techniques such that, even in a case where a plurality of image processing sections having the same functions is provided in parallel, control performed by one control unit for processing in one of the image processing sections allows processing in other image processing sections to be concurrently controlled.

In order to solve a part of the above-described problems, an image-processing apparatus includes n image processing sections which receive n (n represents an integer equal to or larger than "2") consecutive pixel data items that are respectively input with the same timing and which respectively process the respective input pixel data items with the same timing; and a control section for controlling the n image processing sections, wherein each of the image processing sections is capable of being set to one of a first operation mode allowing data communication with the controlling section and a second operation mode allowing only reception from the aforementioned controlling section, one of the image processing sections is set to the first operation mode, and n–1 image processing sections are set to the second operation mode; commands are commonly given to the n image processing sections from the controlling section; and when a command is given from the controlling section to the one of the image processing sections that is set to the first operation mode, the n image processing sections respectively execute the same processing with the same timing.

Page 3, lines 6-9, delete current paragraph and insert therefor:

In the above image-processing apparatus, each of the image processing sections includes a mode-setting terminal for setting one of the first operation mode and the second operation mode, and one of the operation modes is set according to a mode-setting signal input to the mode-setting terminal.

Page 3, line 25, delete current heading and insert therefor:

BRIEF DESCRIPTION OF THE DRAWINGS

Page 3, lines 29-30, delete current paragraph and insert therefor:

Figs. 2(A)-2(C) illustrate processing to be performed by first and second OSDCs 120A and 120B.

Page 4, lines 2-5, delete current paragraphs and insert therefor:

Figs. 5(A) and 5(B) show operation performed between the first and second OSDCs 120A and 120B and a CPU 140.

Figs. 6(A) and 6(B) show an I/O address space and a memory space in the CPU 140.

Page 4, line 11, delete current heading and insert therefor:

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Page 4, lines 13-29, delete current paragraphs and insert therefor:

FIG. 1 is a block diagram showing an outline configuration of an image-displaying apparatus that includes an image-processing apparatus in accordance with a first embodiment of the present invention. An image-displaying apparatus 1000 includes an image-processing apparatus 100 and an image-displaying section 200. The image-processing apparatus 100 is a computer system that includes a scan converter 110 (which is simply referred to as an "SC", hereinbelow), two on-screen display controllers 120A and 120B (each of which is simply referred to as an "OSDC", hereinbelow), an OSD memory 130, and a CPU 140. The image-displaying section 200 includes a liquid crystal panel 210 and a panel-driving section 220. The image-processing apparatus 100 processes images to be formed on the liquid crystal panel 210. The invention also covers a configuration wherein the panel-driving section 220 is provided in the image-processing apparatus 100.

The CPU 140 is connected to the SC 110 and the two OSDCs 120A and 120B via a CPU bus 142. The CPU 140 sets processing conditions of respective sections and directly controls processing performed in the respective sections. The OSD memory 130 is connected to the first and second OSDCs 120A and 120B via a memory bus 132.

Page 5, lines 11-25, delete current paragraphs and insert therefor:

The first and second OSDCs 120A and 120B are image processing sections that each display embellishment images, such as pointer images, and menu screens in images that are displayed in the image-displaying section 200. These first and second OSDCs 120A and 120B correspond to the image processing sections of the present invention. In the OSD memory 130, graphic data and font data that compose image data for pointer images and menu screens are stored in predetermined formats.

Figs. 2(A)-2(C) illustrate processing to be performed by the first and second OSDCs 120A and 120B. In synchronization with the vertically-synchronous signal VD, the clock signal DCLK, and the horizontally-synchronous signal HD, the first OSDC 120A expands the image data read out from the OSD memory 130 so as to be bitmap data, and OSD image data DOD as shown in FIG. 2 (B) is thereby generated. The OSD image data DOD thus generated is combined with the odd-number-pixel image data DSD included in image data DS as shown in FIG. 2(A), and combined odd-number-pixel image data DSODD is thereby output.

Page 7, line 26 - page 8, line 15, delete current paragraphs and insert therefor:

As shown in FIG. 4, when the operation mode is set to the slave mode, the CPU I/F section 350 is controlled so as to be inhibited from outputting data to the data bus DTA and so as to be permitted only to input data thereto. The mode control section 370 is controlled so as to be inhibited from outputting individual data to a memory address bus MADR, a memory data bus MDTA, and a memory control bus MCTL. As described,

however, since a memory control section 340 is set with the same control data as in the case of the memory control section 340 in the first OSDC 120A, it operates with the same timing as in the master mode. Therefore, the second OSDC 120B operating in the slave mode can concurrently retrieve the image-processing data that the first OSDC 120A operating in the master mode has read out from the OSD memory 130.

Figs. 5(A) and 5(B) show operation performed among the first and second OSDCs 120A and 120B and the CPU 140. Figs. 6(A) and 6(B) show an I/O address space and a memory space in the CPU 140. As shown in FIG. 6(A), only an address space for a single OSDC is allocated in the I/O address space in the CPU 140, and the same I/O address is allocated for the two OSDCs 120A and 120B. As described earlier, the first and second OSDCs 120A and 120B have completely the same internal functions except that the different operation modes are set. Therefore, when the CPU 140 requests the first OSDC 120A to input (write) data, as shown in FIG. 5(A), the data is input to the first OSDC 120A, and concurrently, the same data is input to the second OSDC 120B from the CPU 140 via the CPU bus 142 (the CPU address bus ADR, the CPU data bus, and the CPU control bus CTL).

Page 11, lines 5-8, delete current paragraph and insert therefor:

The present invention is not restricted to the above-described examples and embodiments, and the invention may be implemented in various modes without departing from the scope of the invention. A few exemplary modifications are described below. However, the invention is not restricted by the following exemplary modifications.

Page 11, lines 13-27, delete current paragraphs and insert therefor:

(2) In the above-described embodiments, the description has been given with reference to the direct-view type image-displaying section 200 as the example. However,

it may also be a projection-type displaying apparatus using a projection optical system for projecting images.

(3) In the above-described embodiments, the description has been given of exemplary structures that include the plurality of on-screen display controllers arranged in parallel. However, the present invention is not restricted thereto. For example, the invention may be applied to a case where a plurality of various types of image processing sections that perform various types of processing for video signals, such as an image-magnification/reduction processing section and a color-signal-level correcting section, are provided in parallel. Also, in the above-described embodiments, the description has been given of the example image-processing apparatus applied to the image-displaying apparatus. However, the invention is not restricted thereto, and it may be applied to a variety of image-processing apparatuses provided in electronic apparatuses that handle various types of images.

Page 11, delete line 28.

IN THE CLAIMS:

Please replace claims 1-11 as follows:

1. (Amended) An image-processing ~~apparatus, comprising:~~

n image processing sections which ~~receive~~ n (n represents an integer equal to at least "2") consecutive pixel data ~~items~~ that are respectively input with the same timing and which respectively process the respective input pixel data items with the same timing; and

a control section that controls the n image processing sections;

wherein each of the image processing sections are capable of being set to one of a first ~~operation mode allowing~~ data communication with the control section, and a second operation mode allowing only reception from ~~the control section~~, one of the image